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Aligned Fusion Wafer Bonding for CMOS-MEMS and 3D Wafer-Level Integration Applications

V. DRĂGOI[1], G. MITTENDORFER[1], C. FLÖTGEN[1],
D. DUSSAULT[2], T. WAGENLEITNER[1]

[1]EV Group, DI E. Thallner 1, 4782 - St. Florian/Inn, Austria
E-mail: v.dragoi@evgroup.com
[2]Product Systems Inc., 1745 Dell Av., Campbell, CA 95008, USA

Abstract. Wafer bonding proved to be a valuable MEMS manufacturing technology during past years, when bonding-based applications moved to high volume production. Due to its ability to allow for building 3D architectures wafer bonding became very attractive also for applications using wafer-level 3D integration. However, most of the bonding processes are not compatible with CMOS technology in terms of process temperature and contamination levels. A low temperature fusion bonding process is presented as an example of how the wafer bonding issues were successfully solved and applied to manufacturing processes.

Keywords: plasma activated wafer bonding, single wafer cleaning, optical alignment, CMOS image sensor, back-side illumination, 3D integration.

1. Introduction

Wafer bonding is a well established technology for Micro- Electro- Mechanical Systems (MEMS) applications and wafer-level packaging. The increased complexity of new generations of MEMS for consumer products applications raised new challenges for wafer bonding process by moving from mainly blank or surface machined wafers to bonding of wafers with electronic functionality. In parallel a significant effort is focused on wafer-level 3D integration as a viable solution for increasing functionality and overcome the wire bonding bottle neck in terms of components density and size.

Complementary Metal-Oxide-Semiconductor (CMOS) is a standard technology used in microprocessors, microcontrollers, Random Access Memories (RAM) as well as for analog circuits such as CMOS image sensors (CIS), analog to digital converters and integrated transceivers for communication.

The use of CMOS wafers imposes important limitations for W2W (Wafer-to-Wafer): low temperature (max. 400°C), no mobile ions and extreme particle cleanliness. Process temperature condition eliminates practically all high temperature wafer bonding processes as silicon fusion bonding requiring temperatures between 700°C – 1100°C [1]. The low metal ions traces values acceptable further exclude processes as the robust anodic wafer bonding due to its high level of Na ions contamination. By considering the low contamination criteria the area of CMOS-compatible bonding processes is further reduced.

Even with the aforementioned restrictions there are still several different bonding processes which are compatible with CMOS technology:

- Low temperature fusion (direct) bonding;
- Eutectic or Transient Liquid Phase (TLP) wafer bonding (*e.g.* Al-Ge);
- Metal thermo-compression bonding (*e.g.* Cu-Cu, Al-Al);
- Adhesive wafer bonding with polymers.

Low temperature plasma activated fusion bonding can be used for 3-dimensional (3D) wafer-level integration applications and for Back-side Illuminated (BSI) CMOS image sensors.

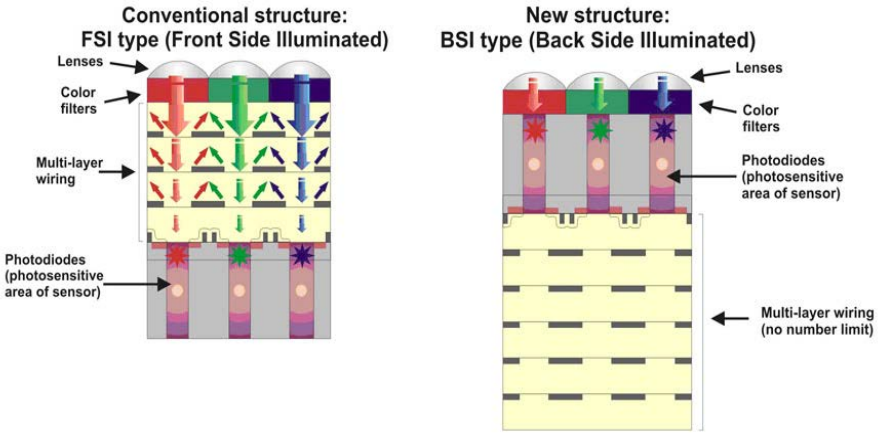

Fig. 1. Schematic illustration of Front-Side and Back-Side Illuminated CMOS image sensors functional principle.

Through-Silicon Vias (TSV) technology was adopted during past years for building 3D architectures by stacking fully processed wafers. In this technology there are two main approaches: "via-first" and "via-last". In the first approach, wafers with TSVs already completed are optically aligned and finally bonded using a bonding process

which provides simultaneously mechanical and electrical connection between the metal pads from the surfaces of the two wafers (usually a metal thermo-compression bond).

In the "via-last" approach wafers are first bonded, then one wafer is thinned (typically by grinding and polishing), then vias are etched and filled with metal. Optically aligned plasma activated fusion bonding can be used for such bonding process.

The new CMOS image sensors technological approach of Back-Side Illumination (BSI) *vs.* classical approach using Front-Side Illumination (FSI) is shown in Fig. 1. With the FSI approach challenge of the pixel area limitation due to an overlap of the optical path with electrical interconnects, the new BSI technique consists of a separation between the two, thus resulting in no influence of the CMOS metal layers (electrical interconnects) on the optical path.

In terms of process flow, the BSI image sensor is built in CMOS technology starting with the photodiode and building the electric circuitry on top of it (Fig. 2).

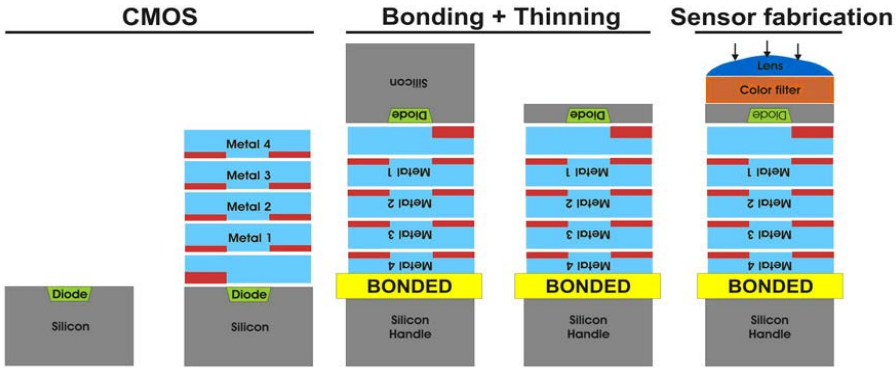

Fig. 2. Schematic process flow of BSI CMOS image sensor.

After sensor fabrication process is completed the opening of the photodiode to light is needed, followed by additional process steps required for integrating the color filters and lenses.

This paper presents results on surface preparation (cleaning and activation), high-accuracy optical alignment and strong, defects-free, CMOS-compatible bonding process.

2. Experimental

2.1. Wafer Cleaning

The CMOS technology has very strict requirements in terms of various types of contamination: particles, metal traces and organic. Cleaning processes for wafer bonding are based on wet chemical procedures (*e.g.* Standard Cleaning1 and Standard Cleaning2 – SC1 + SC2) which can ensure the desired particles, organic and metal traces levels.

However, in wafer bonding an additional single wafer cleaning step is often used in order to remove particles potentially trapped on wafers' surfaces during wafers handling between cleaning wet bench and wafer bonding equipment. Typically this final cleaning is based only on water cleaning and only rarely some diluted chemicals (*e.g.* 2% of NH_4OH) are used in order to enhance particle removal efficiency. This step was traditionally performed using brush scrubbing or megasonic nozzles. Due to cleaning uniformity concerns in case of megasonic nozzles or due to the ross contamination concerns in case of brushes, a new megasonic transducer was developed: MegPie® [2]. Due to its triangular shape (Fig. 3) this ensures uniform radial distribution of the acoustic energy across wafer. The transducer is placed in close proximity and the gap between wafer surface and transducer surface have to be filled with liquid.

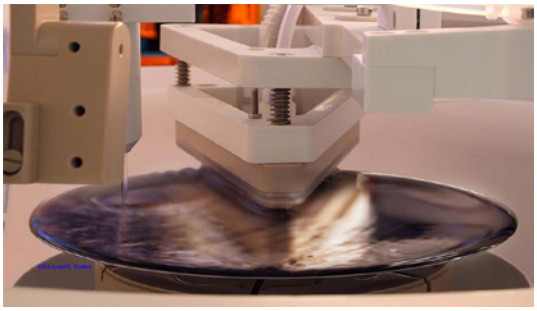

Fig. 3. MegPie® transducer in cleaning process.

2.2. Surface Preparation

CMOS wafer requires special surface preparation in order to be compliant with direct bonding requirements. The most used technique for CMOS wafer planarization is a combination of silicon oxide deposition and Chemical Mechanical Polishing (CMP). Due to the fact oxide deposition is a conformal process, multiple oxide deposition-CMP cycles may be required.

After deposition, the silicon oxide is densified by a thermal annealing. This step is very important for removing residual gas trapped in the oxide layer during PECVD. Without this step usually the trapped gas will accumulate at the interface forming large voids at the bonded interface. Ideally, the densification temperature value is in the same range with wafer bonding thermal annealing.

After densification, the PECVD oxide layer has to be polished using CMP. Plasma activated wafer bonding gives with very good results for surface microroughness $<$0.5 nm, good results for microroughness $<$1 nm and still possible (under certain special conditions) for microroughness $<$1.5 nm. Microroughness is usually defined as the Rms of a surface measured by Atomic Force Microscope (AFM) on 2×2 μm^2 area.

After CMOS planarization the wafers are plasma activated [3], optically aligned, pre-bonded (placed in contact) in the optical aligner at room temperature and then thermally annealed in a batch process at temperatures of maximum 400°C.

2.3. Wafer-to-Wafer Alignment

Before bringing the wafers in contact at ambient conditions the wafers have to be precisely aligned. For this type of application an alignment method was introduced, which uses single side processed wafers (Fig. 4).

In this alignment approach two pairs of microscopes are used to track the alignment keys on the two wafers. The alignment method is an indirect one, meaning the two wafers are not aligned using live view of the alignment keys, but using the digitized images of the two wafers stored with respect to a reference point. A high precision mechanical stage allows reaching alignment accuracies below 500 nm for wafers size up to 300 mm diameter [5].

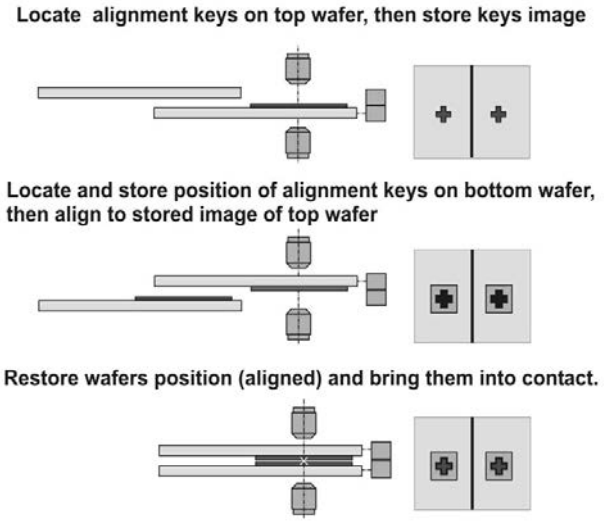

Fig. 4. SmartView® NT wafer-to-wafer optical alignment principle [4].

2.4. Wafer-to-Wafer Bonding

After planarization the wafers have to be activated in order to allow a low temperature process. This process is performed by activating the wafers in a plasma chamber [3].

In this process, wafers are exposed to a nitrogen plasma before loading them into the optical aligner. By contrast with numerous literature reports on plasma activated bonding, the process employed here does not require rinsing of the two surfaces between plasma activation and bonding in order to increase bond strength [6].

The two wafers are placed in contact at ambient conditions inside the optical alignment equipment.

3. Results

The compatibility of the above described processes for fusion bonding of CMOS wafers was studied.

3.1. Wafer Cleaning

The maximum levels of contaminants allowed for CMOS manufacturing process are shown in Table 1.

Table 1. Contamination levels allowed in CMOS manufacturing (adapted from [7])

Parameter	**Device Critical Dimensions [µm]**				
	0.65	**0.5**	**0.35**	**0.25**	**0.15-0.10**
Particles					
Size [µm]	0.3	0.16	0.11	0.08	0.05
Density (target/limit) [cm^{-2}]	0.03/0.09	0.06/0.10	0.05/0.10	0.04/0.08	0.02/0.05
Contamination levels					
Ionic species [cm^{-2}]	$<10^{11}$	$<10^{10}$	$<10^{9}$	$<10^{8}$	$<10^{7}$
Transition metals [cm^{-2}]	$<10^{12}$	$<10^{11}$	$<10^{10}$	$<10^{9}$	$<10^{8}$

Silicon wafers, 200 mm diameter, were intentionally contaminated using silicon nitride particles with different sizes, then cleaned using MegPie® with deionized water.

A high particle removal efficiency was obtained, compatible with fusion wafer bonding requirements (Fig. 5).

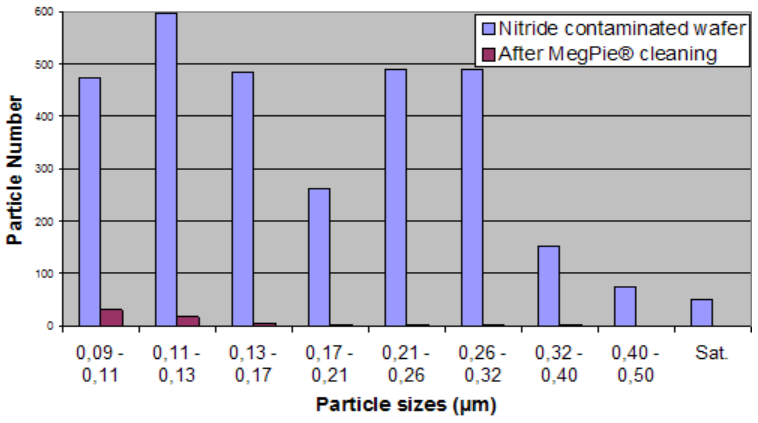

Fig. 5. Particle size distribution before and after MegPie® cleaning of a silicon wafer intentionally contaminated with silicon nitride particles [8].

3.2. Wafer-to-Wafer Alignment

In order to check the maximum alignment accuracy reachable, 300 mm silicon wafers with defined alignment keys were aligned with glass wafers having complementary alignment keys. After each alignment process the wafers were placed in contact, clamped, and alignment accuracy was measured. The process was repeated for 400 times in a marathon run in order to check reproducibility and equipment stability.

Results are shown in Fig. 6.

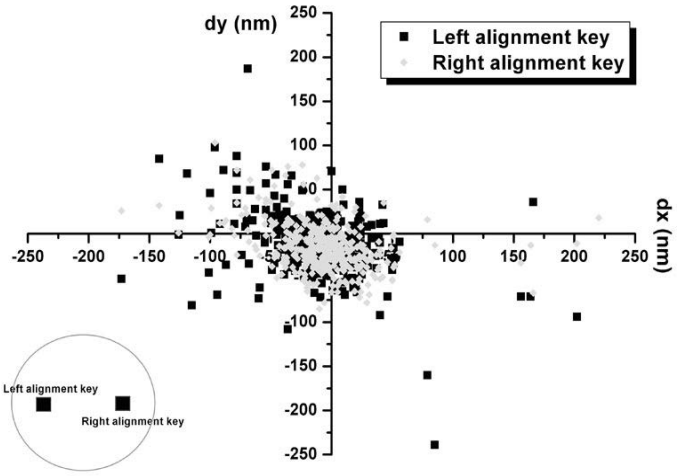

Fig. 6. Alignment accuracy data (dx and dy misalignment) recorded for 400 consecutive alignment procedures.

It can be observed that most of the alignment results are within 150 nm and better accuracy, which makes the process compatible with 3D integration applications.

3.3. Wafer-to-Wafer Bonding

Wafer bonding process was first qualified for blank silicon wafers in order to determine the plasma activation condition providing high bond strength. Process was optimized to reach bond strength in the same range with silicon bulk fracture strength at annealing temperature of 250°C – 350°C for 1–3 hours [3].

After determining the optimum plasma activation condition, the CMOS planarization sequence was optimized.

The acoustic microscope image in Fig. 7 shows a bonded CMOS wafer pair. There is no unbonded area visible across the bonded pair (bonded area shown by black color, white color shows unbonded areas), only a small defect (white dot) is visible at the edge (the right side of the image). With such a high bonding quality in terms of defects and bond strength, CMOS wafer bonding is possible.

Fig. 7. Scanning Acoustic Microscope image of a 200 mm diameter CMOS wafer bonded to a blank Si wafer.

4. Conclusions

New processes were developed for accommodating the requirements raised by CMOS technology to wafer bonding.

An innovative single wafer megasonic cleaning process (MegPie®) was developed to meet the particle removal efficiency and high uniformity required by current CMOS applications. Partical neutrality and high particle removal efficiency were demonstrated.

Optical alignment accuracy of less than 200 nm was achieved using a face-to-face alignment method in the new generation of SmartView® NT optical alignment equipment. The same equipment is used to place the two wafers in contact after alignment for fusion bonding without introducing any stress.

Plasma activated fusion wafer bonding was optimized to ensure a dry process (no water or chemicals rinse required between plasma activation and bonding) resulting in high bond strength with short process times compatible with high volume manufacturing requirements.

The process features described in this paper are currently in use for BSI CMOS image sensors for use in mobile phones and other consumer products and for "via-last" 3D integration applications.

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